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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/820,243	03/28/2001	Terry L. Kendall	42390P10070	3769

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EXAMINER	
PORTKA, GARY J	

ART UNIT	PAPER NUMBER
2188	19

DATE MAILED: 05/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/820,243	Applicant(s) KENDALL, TERRY L.	
	Examiner Gary J Portka	Art Unit 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,21,23 and 25-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,21,23,29,30,35 and 36* is/are rejected.

7)☒ Claim(s) *25-28 and 31-34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 22, 2004 has been entered.

2. Claims 1, 3-4, 6, 8-9, 21, and 23 have been amended, and claims 25-36 have been added by Applicant. Claims 1-9, 21, 23, and 25-36 are pending.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-9, 29-30, and 35-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor et al., U.S. Patent 6,263,398 B1, in view of Martinez, Jr. et al., U.S. Patent 5,596,731.

5. As to claims 1 and 6, Taylor discloses the recited memory device integrated with cache (see Abstract, Figure 1, and column 3 lines 7-35), and stores recently accessed data at 14 and associated addresses at 24. Taylor also additionally teaches a wait

control signal, see signal READY 32 in Fig. 1, and described at col. 5 lines 19-24 and 56-62. The READY signal is asserted for a cache hit (see col. 6 lines 55-62) and for a cache miss (see col. 7 lines 10-37). It is clear from col. 5 lines 21-24 that the READY signal may be active high or active low. It follows that the inactive state of the signal may be considered a wait control signal. In the miss case it is certain that it takes multiple clock cycles to assert the READY signal, and thus Taylor teaches the recited wait control signal of multiple cycles when data is not in the cache. In the hit case, it is not clear that the READY signal is asserted within one cycle, only that a cache hit should provide the data faster than the non-volatile memory would. Therefore, Taylor does not teach a wait control signal of one cycle when data is in the cache. However, it was known to be desirable to have the capability of providing data from a cache within one clock cycle, and Martinez teaches such a system, which as in Taylor provides a signal when data is ready, and within one cycle when a cache hit occurs (see Martinez col. 2 lines 41-54, and col. 9 lines 24-43). An artisan would have desired this one cycle hit speed in the system of Taylor. It therefore follows from the above that an artisan would have desired and would have known how to implement a wait control signal of one clcok cycle from the time of an access request, for a cache hit. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use a wait control signal of one clock cycle when the data is in the cache in Taylor, because this is the same as asserting the READY signal within one clock cycle of an access request, and Martinez had taught that for a cache hit data may be ready within one cycle for the maximum access speed.

6. As to claims 2-4 and 7-9, Taylor discloses address latch logic 18, 20, address cache and comparison at 24, and data cache 14. See Fig. 1 and col. 4 lines 56-66, and col. 5 lines 60-62. The data is allowed to be read in the next cycle since when there is a hit in the cache (Fig. 4, 314) the ready signal is immediately indicated (316).

7. As to claim 5, the address is not presented to the memory as recited since when there is a cache hit the column address is applied directly to the cache (see col. 8 lines 32-36).

8. As to claims 29-30 and 35-36, neither Taylor nor Martinez disclose receiving the address without two least significant bits, and comparison without those bits. However, since only the row is compared, and some number of bits is required for the column address, this choice is a trivial case of using two bits for the selection between four columns. It is further noted it is trivial to identify any particular bits as least significant if this is not related in any other way to other claim elements. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to not use the two least significant bits of the address, because the is the result of using bits from one selected end of an address for the purpose of selecting between four columns.

9. Claims 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor et al., U.S. Patent 6,263,398 B1, in view of Martinez, Jr. et al., U.S. Patent 5,596,731, and further in view of Sakamoto, U.S. Patent 6,288,923 B1.

10. As to claims 21 and 23, neither Taylor nor Martinez describe the recited quadwords. However, such quadwords were well known in the art; for the clear benefit of simplifying and/or reducing the complexity of the circuitry or steps required to access

four consecutive words. Sakamoto discloses quadwords to the extent recited. See Figures 6-10, where data is output in groups of four registers. Multiple and non-consecutive quadwords are stored simultaneously in the register array shown in Figure 4. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use the recited quadwords, because these were known in the art as an efficient means of transferring four consecutive words.

Allowable Subject Matter

11. Claims 25-28 and 31-34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

12. Applicant's arguments filed March 22, 2004 have been fully considered but they are not persuasive.

Applicants argue that Taylor does not teach a wait control signal. Examiner disagrees, and maintains that the READY signal in Taylor is, as described hereinabove, in effect defined as the opposite state of a wait control signal, and therefore serves the same function. Applicant argues that Taylor does not contain an address cache and comparator, but Examiner disagrees and maintains that item 24 is an address cache and comparator to the extent claimed since it determines if the address and associated data is in the cache 14, and cause assertion of the READY signal if so (see col. 6 lines 56-62).

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Patent No:

5,787,486 Data ready strobe from cache if a hit and from controller if a miss.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary J Portka whose telephone number is (703) 305-4033. The examiner can normally be reached on M-F 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 305-3900.

Gary J Portka
Primary Examiner
Art Unit 2188

May 3, 2004